REMARKS/ARGUMENTS

Claims 1-9 are currently pending in this application. Claims 1-4 have been amended for clarity without further limitation. In view of the above amendments and following remarks, applicants respectfully submit that the application is in condition for allowance. Applicants therefore, respectfully request reconsideration and allowance of the application.

The Examiner rejected claims 1-9 under 35 U.S.C. 103(a) as being obvious over Porterfield (U.S. Patent 6,141,715) in view of Alzien et al., (U.S. Patent 5,987,555). The Examiner alleges that Porterfield discloses identifying a target requested by a master and determining if data associated with the target is available. The Examiner admits that Porterfield fails to disclose assigning priority for ownership of the PCI bus to the master based on availability of data. The Examiner alleges however that Alzien discloses that once the data is available the PCI arbiter provides a level of arbitration priority to the PCI master. Applicant respectfully traverses this rejection.

Independent claim 1 recites a method for assigning ownership of a peripheral component interconnect (PCI) bus comprised in part by "determining if data associated with the target is available; and assigning a first priority level for ownership of the PCI bus to the master if the data is not available and assigning a second priority level for ownership of the PCI bus to the master if the data is available." Applicants respectfully submit that the cited references, alone or in combination do not disclose or suggest the recited limitation.

Rather, Porterfield discloses a computer system having a PCI-host bridge 16 that includes a memory buffer 38 having a write buffer 39 that "temporarily stores data being transmitted

to and from the memory 18 via the memory interface 32." (Porterfield, col. 4, lines 10-14). The system of Porterfield then grants ownership of the bus based upon availability of space in the write buffer. For example, to process write transaction requests the Porterfield system "determines whether the write buffer 39 is full. If the write buffer 39 is not full, then … the write transaction request is executed normally … If the … write buffer 39 is full, then … the PCI target interface 34 transmits a retry command to the bus master that submitted the current transaction request." (Porterfield, FIG. 4, col. 6, lines 13-31).

Similarly if the current transaction request is not a write transaction request, then the Porterfield system "determines whether the write buffer 39 is empty … If the write buffer 39 is empty, then … the current read transaction request is executed normally … If … the write buffer is not empty, then … the PCI target interface 34 transmits a retry command to the bus master that submitted the current transaction request." (Porterfield, FIG. 4, col. 6, lines 39-52).

In both instances Porterfield avoids "livelock conditions on the PCI bus 20 by preventing any transaction requests from any of the bus masters other than a first bus master, from being processed until a re-submitted transaction request from the first bus master is processed in the event the transaction request could not be processed the first time it was submitted by the first bus master." Porterfield, col. 4, lines 56-64).

Thus Porterfield assigns ownership of the bus based upon availability of space in the write buffer. Porterfield does not

however disclose or suggest determining if data associated with the target is available; and assigning a first priority level for ownership of the PCI bus to the master if the data is not available and assigning a second priority level for ownership of the PCI bus to the master if the data is available as recited in claim 1 of the present invention.

Similarly, in the system of Alzien when a delayed read operation is established by a particular PCI master, "bridge logic unit 102 provides an indication to the PCI arbiter 804 indicating the pending delayed read operation. PCI arbiter 804 responsively prevents the PCI master from obtaining ownership of PCI bus 114. When the delayed read data is obtained and available in transient read buffer 416, bridge logic unit 102 provides a further indication to PCI arbiter 804, which responsively provides a normal level of arbitration priority to the PCI master to allow the reattempted read operation." (Alzien, col. 23, lines 13-22; underlining added for emphasis only).

Thus, the system of Alzien completely prevents the PCI master from gaining ownership of the bus if a delayed read is indicated and provides a normal level of arbitration priority only when the data is available. Alzien does not however determine if data associated with the target is available and assign a first priority level for ownership of the PCI bus to the master if the data is not available and assign a second priority level for ownership of the PCI bus to the master if the data is available as recited in claim 1 of the present invention (underlining added for emphasis only).

Applicants therefore respectfully submit that claim 1 recites a novel and unobvious method over the cited references and is therefore allowable. Applicants further submit that claims 2-9 that depend directly of indirectly from claim 1 are allowable as is claim 1 and for additional limitations recited therein.

It is therefore respectfully submitted that pending claims 1-9 are in condition for allowance, and an early notice of allowance is respectfully requested.

Respectfully submitted,
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